Docket No.: P2001,0097



# CERTIFICATION

I the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of the German Patent Application 101 06 556.6, filed February 13, 2001.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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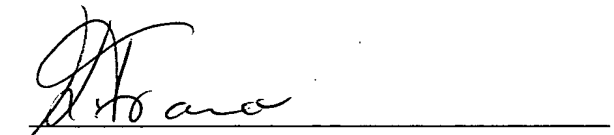

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# SEMICONDUCTOR MODULE WITH AN ARRANGEMENT FOR THE SELF-TEST OF A PLURALITY OF INTERFACE CIRCUITS AND TEST METHOD

The present invention relates to a semiconductor module with a plurality of interface circuits and an arrangement for the self-test of interface circuits. The application furthermore relates to a method for the self-test of interface circuits of such a semiconductor module.

All semiconductor modules communicate with other devices via I/O interface circuits. With fast interface circuits, for example LVDS (Low-Voltage Differential Signals) or DDR (Double Data Rate), the necessary functional tests require a very high accuracy with regard to timing control and voltage.

The most widespread test method uses external test systems having very high accuracy with regard to timing control and voltage, which are connected via a multiplicity of signal lines to the modules to be tested. However, this procedure is increasingly encountering its limits, since test systems having the high accuracy required for the present-day fast interface circuits are very costly and in some instances are not commercially available with the required specification.

One possibility for dispensing with an external test system consists in providing an on-chip test logic with PLL (Phase-Locked Loop) or DLL (Delay-Locked Loop). However, this procedure is very complex and requires a very large chip area for the integration of the high-precision PLL or DLL test logic.

This marks the starting point for the invention. The invention, as characterized in the claims, is based on the object of specifying a method enabling fast interface circuits of semiconductor modules to be tested reliably and with a low outlay. This object is achieved by means of the semiconductor module according to claim 1 and the method for the self-test of interface circuits according to claim 7.

According to the invention, a semiconductor module with a plurality of interface circuits has an arrangement for the self-test of interface circuits, which comprises:
- two equally sized groups of interface circuits such that each interface circuit of the first group is assigned exactly one interface circuit of the second group,
- a circuit which interacts with the first group and serves for generating test signals which can be output via the interface circuit of the first group;
- a circuit which interacts with the second group and serves for receiving and processing test signals received via the interface circuits of the second group, so that a connection of the assigned interface circuits of the first and second groups enables a self- test,
the first and second groups of interface circuits having a separate voltage supply.

The invention is thus based on the concept of utilizing the interface circuits for testing themselves. To that end, the interface circuits are divided into two groups and test signals are output via the first group of interface circuits. Via an external connection of the first group to the second group of interface circuits, during the self- test, the test signals pass to the second group of interface circuits, where the test signals are received and processed in a circuit.

In this case, the separate voltage supply of the first and second groups of interface circuits allows good test coverage by separate variation of the voltage of transmitting and receiving group.

Preferably, the semiconductor module further has a circuit which interacts with the second group and serves for generating test signals which can be output via the interface circuit of the second group, and a circuit which interacts with the first group and serves for receiving and processing test signals received via the interface circuit of the first group. As a result, it is possible to test both groups of interface circuits, each group occurring on one occasion as transmitter and on one occasion as receiver of the test signals.

The circuit or the circuits for generating test signals advantageously comprise a pseudorandom number generator, in particular a linear feedback shift register (LFSR).

The circuit or the circuits for receiving and processing test signals advantageously comprise a circuit for calculating a signature from the test signals, in particular a multiple input shift register (MISR).

During the self-test of the interface circuits of such a semiconductor module, the assigned interface circuits of the first and second groups are connected to one another, the two groups are supplied with a separate supply voltage, test signals are generated and output via the first group of interface circuits, the test signals are received via the second group of interface circuits, and the received test signals are compared with prescribed values for fault-free functioning of the interface circuits.

Preferably, both groups have a circuit for generating test signals, so that, after the processing of the test signals output by the first group and received by the second group of interface circuits, the test direction can be rotated. Then, the test signals generated by the circuit which interacts with the second group are output via the second group of interface circuits and are received via the first group of interface circuits, and the received test signals are compared with prescribed values for fault-free functioning of the interface circuits.

In a preferred refinement, the connection paths of the assigned interface circuits are influenced resistively, capacitively or inductively during testing, in order to increase the test coverage by including interference quantities in the self-test.

Furthermore, a low-frequency signal voltage can be modulated onto at least one of the supply voltages of the interface groups. Preferably, low- frequency sinusoidal signals of different frequency are modulated onto both supply voltages, thereby achieving a timing test which is very close to the application and even goes beyond the possibilities of an external test system.

Overall, the invention described permits a relatively short test time without necessitating high- precision test systems with regard to the timing control or voltage. The customary mismatch when the high- speed pins are capacitively coupled to the test system is obviated. Moreover, only a small additional hardware outlay arises on the semiconductor module, since no PLL or DLL logic is required.

In a production test, the test method described is expediently used after the packaging of the chips, since the boards are better suited to this than needle cards.

Further advantageous refinements, features and details of the invention emerge from the dependent claims, the description of the exemplary embodiments and the drawings.

The invention will be explained in more detail below using exemplary embodiments in connection with the drawings. Only the elements essential to the understanding of the invention are illustrated in each case. In the figures:

Figure 1 shows a schematic illustration of an exemplary embodiment of the invention in a test with a DUT board;

Figure 2 shows a schematic illustration of another exemplary embodiment of the invention in a test with a needle card;

Figure 3 shows a schematic illustration of a further exemplary embodiment of the invention in a test with a DUT board.

Figure 1 shows a semiconductor module 10 with a logic core 36 and I/O interface circuits 12a, 12b, 14a, 14b, which are assigned terminal pads 22a, 22b, 24a, 24b on the semiconductor module. In this case, in order to make the illustration easier to understand, the schematic illustration of figure 1 shows only four I/O interface circuits, whereas in real devices the number of I/O interface devices is generally greater than four, for example 16 or 32.

The interface circuits 12a - 14b are divided into a first group, containing the interface circuits 12a and 12b, and a second group, containing the interface circuits 14a and 14b.

The two groups each have a separate voltage supply. Although all the interface circuits 12a - 14b share the negative supply voltage VSSP (reference symbol 16), the positive supply voltage VDDP1 (reference symbol 18) and VDDP2 (reference symbol 19) is respectively separate for the two groups and embodied via separate terminal pads 28, 29 on the semiconductor chip 10.

Each group of interface circuits is connected to a linear feedback shift register LFSR (reference symbols 32a, 32b and 34a, 34b, respectively) for generating pseudorandom-distributed test signals. Furthermore, both groups of interface circuits are connected to the common multiple input shift register (MISR) 30. The MISR 30 calculates from received test signals a signature which can be used for checking the correct reception of the test signals.

In the housed state, the semiconductor module 10 is situated in a package 40, the terminals of the interface circuits being routed out at pins 42 - 49 of the package. The supply voltage 38, 39 for the logic core 36 is additionally provided.

For the self-test, the semiconductor module 10 is connected to a DUT (Device Under Test) board 50. The DUT board 50 contains a connection 52, which connects the pin 42a to the pin 44a of the package and thus the interface circuit 12a to the interface circuit 14a. In the same way, the connection 54 connects the pins 42b and 44b of the package and thus the interface circuits 12b and 14b.

During test operation, first of all the LFSR 34a, 34b generates a series of test signals which are output via the interface circuits 14a, 14b and pass via the connections 52, 54 to the interface circuits 12a, 12b and from there to the

MISR 30, which calculates a signature from the test signals. After a specific number of received test signals, the calculated signature is compared with a prescribed signature for fault- free functioning of the interface circuit.

Afterward, the test direction is rotated, that is to say the LFSR 32a, 32b then generates test signals which are output via the interface circuits 12a, 12b, are received via the connections 52, 54 and the interface circuits 14a, 14b and pass to the MISR 30 for evaluation.

In order to achieve high test coverage, the test is multiply iterated and the voltage at the separate power supplies 18, 48 and 19, 49, respectively, for the two interface halves is varied in the process. The separate power supply allows, for example, transmission at high voltage on one half of the interface circuit and reception on the other half of the interface circuit at low voltage.

Furthermore, via the switches 56a, 56b of the DUT board, the connections 52, 54 can be influenced in a targeted manner with interference quantities, with capacitive interference in the exemplary embodiment of figure 1. Instead of the capacitors C, the connections 52, 54 can also be influenced inductively or resistively with impedances or resistors.

Figure 2 shows an LVDS (Low-Voltage Differential Signals) interface as a further exemplary embodiment. The semiconductor module 100 contains a logic core 136 with supply voltage terminals 138, 139, and two LVDS pad pairs 122a, 122b and 124a, 124b, which each belong to an LVDS input 112 and an LVDS output 114, respectively. Here, too, the number of just two interface circuits is not intended to be a limitation, but rather is chosen merely for the sake of simpler illustration.

Both interface circuits 112, 114 have a common negative supply voltage VSSP (reference symbol 116) but a separate positive supply voltage VDDP1 (reference symbol 128) and VDDP2 (reference symbol 129), respectively. The LVDS output 114 is connected to an LFSR 132 for generating test signals, and the LVDS input 112 is connected to an MISR 130 for calculating a signature from the received test signals.

A test with separated supply voltage can only be effected on the wafer in the case of the semiconductor module 100, since the housed semiconductor module has only a single VDDP pin 148 for the positive supply voltage on the package 140 (figure 3). During the test on the wafer, the semiconductor module 100 is tested by means of a needle card 150. The latter contains connections 152, 154, which connect the corresponding pads 122a, 122b and 124a, 124b of the LVDS input 112 and LVDS output 114 to one another.

The connections can again be influenced capacitively, inductively or resistively via switches 156. In addition, figure 2 shows the possibility of modulating different low-frequency sinusoidal signals U1 and U2, respectively, on the two supply voltages. During the fast self- test, the fast frequency is provided by the PLL of the module 100 itself. Comprehensive test coverage is achieved by virtue of the modulated supply voltage fluctuations U1, U2 in combination with the PLL jitter that is really present. In this case, the LFSR/MISR circuit is situated upstream of the multiplexer circuit in the slow frequency range and is simple to realize.

After the separation and packaging the two supply voltage pads 128, 129 in the package 140 are externally accessible only through a single pin 148, so that it is then not possible to

effect the self- test with a separated supply voltage (figure 3). However, a self- test is possible here, too, with a DUT board 250 in the manner described in connection with figure 1.

Patent Claims

1. A semiconductor module with a plurality of interface circuits and an arrangement for the self-test of interface circuits, which comprises
- two equally sized groups of interface circuits (12a, 12b, 14a, 14b; 112, 114), such that each interface circuit of the first group (12a, 12b; 112) is assigned exactly one interface circuit of the second group (14a, 14b; 114),
- a circuit (32a, 32b; 132) which interacts with the first group (12a, 12b; 112) and serves for generating test signals of the first group (12a, 12b; 112) via the interface circuits;
- a circuit (30; 130) which interacts with the second group (14a, 14b; 114) and serves for receiving and processing test signals so that a connection (52, 54; 152, 154) of the assigned interface circuit of the first and second group a self test enables,
with the first and second group of interface circuits show a separate voltage supply (18, 19; 118, 119).

2. The semiconductor module as claimed in claim 1, which further has
- a circuit (34a, 34b) which interacts with the second group (14a, 14b; 114) which serves for generating test signals via the interface circuits of the second group (14a, 14b; 114); and
- a circuit (30) which interacts with the first group (12a, 12b; 112) and serves for receiving and processing test signals received via the interface circuits of the first group (12a, 12b; 112).

3. The semiconductor module as claimed in claim 1 or 2, in which the circuit or the circuits for generating test signals

comprise a pseudorandom number generator (32a, 32b, 34a, 34b; 132).

4. The semiconductor module as claimed in one of the preceding claims, in which the circuit or the circuits for generating test signals comprise a linear feedback shift register (32a, 32b, 34a, 34b; 132).

5. The semiconductor module as claimed in one of the preceding claims, in which the circuit or the circuits for receiving and processing test signals comprise a circuit (30; 130) for calculating a signature from the test signals.

6. The semiconductor module as claimed in one of the preceding claims, in which the circuit or the circuits for receiving and processing test signals comprise a multiple input shift register (MISR) (30; 130).

7. A method for the self-test of interface circuits of a semiconductor module as claimed in one of the preceding claims, comprising the method steps of
- connecting the assigned interface circuits of the first and second groups of interface circuits;
- supplying the two groups of interface circuits with a separate supply voltage;
- generating test signals and outputting the test signals via the first group of interface circuits;
- receiving the test signals via the second group of interface circuits, and
- comparing the received test signals with prescribed values for fault-free functioning of the interface circuits.

8. The method as claimed in claim 7 for the self-test of interface circuits of a semiconductor module as claimed in one of claims 2 to 6,
in which, after the processing of the test signals output by the first group and received by the second group of interface circuits, the test direction is rotated,
such that the test signals generated by the circuit which interacts with the second group are output via the second group of interface circuits and are received via the first group of interface circuits, and the received test signals are compared with prescribed values for fault-free functioning of the interface circuits.

9. The method as claimed in claim 7 or 8, in which test signals with pseudorandom distribution are generated, a signature is calculated from the received test signals, and the signature is compared with a prescribed signature for fault-free functioning of the interface circuits.

10. The method as claimed in one of claims 7 to 9, in which the connection of the assigned interface circuits is influenced resistively, capacitively or inductively in order to include the influence of interference quantities in the self-test.

11. The method as claimed in one of claims 7 to 10, in which low-frequency signal voltages are modulated onto at least one of the supply voltages of the interface groups.

12. The method as claimed in claim 11, in which two low-frequency sinusoidal signals of different frequency are modulated onto both supply voltages.

Abstract

A semiconductor module with a plurality of interface circuits has an arrangement for the self-test of interface circuits, which comprises
- two equally sized groups of interface circuits (12a, 12b, 14a, 14b) such that each interface circuit of the first group (12a, 12b) is assigned exactly one interface circuit of the second group (14a, 14b),
- a circuit (32a, 32b) which interacts with the first group (12a, 12b) and serves for generating test signals which can be output via the interface circuits of the first group (12a, 12b);
- a circuit (30) which interacts with the second group (14a, 14b) and serves for receiving and processing test signals received via the interface circuits of the second group (14a, 14b), so that a connection (52, 54) of the assigned interface circuits of the first and second groups enables a self-test, the first and second groups of interface circuits having a separate voltage supply (18, 19). This enables good test coverage by separate variation of the voltage of transmitting and receiving group.

Figure 1

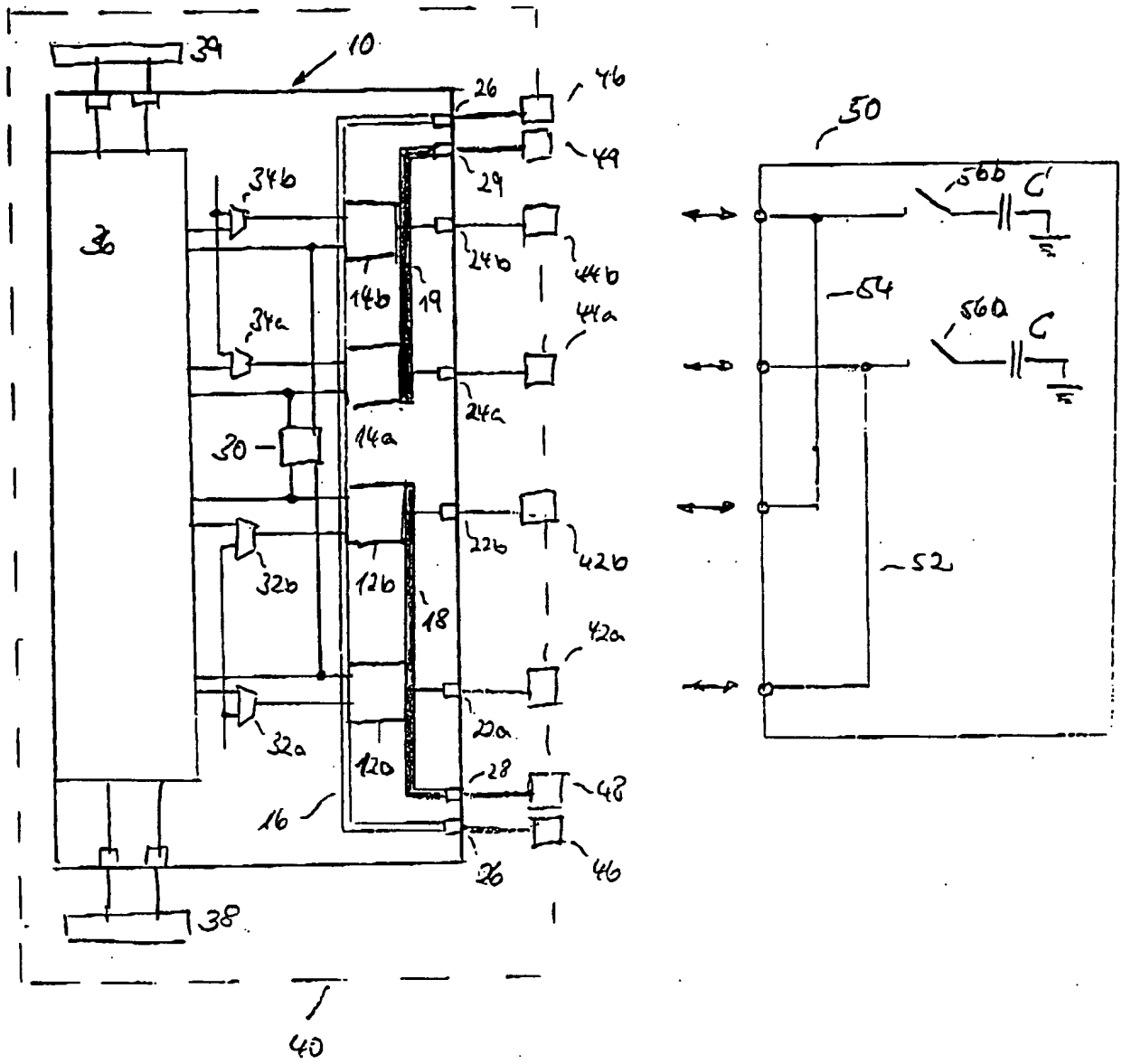


Fig 1

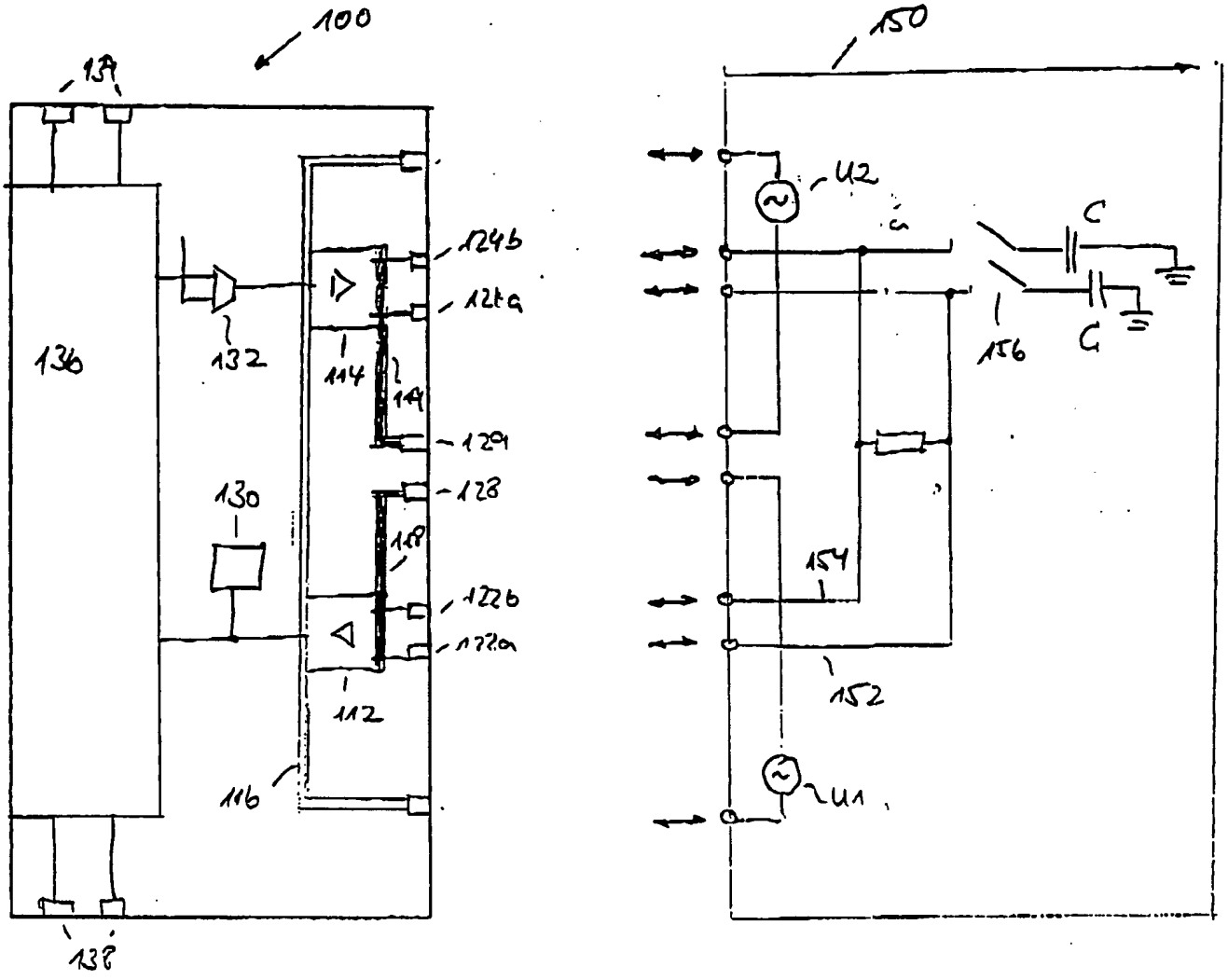


Fig 2

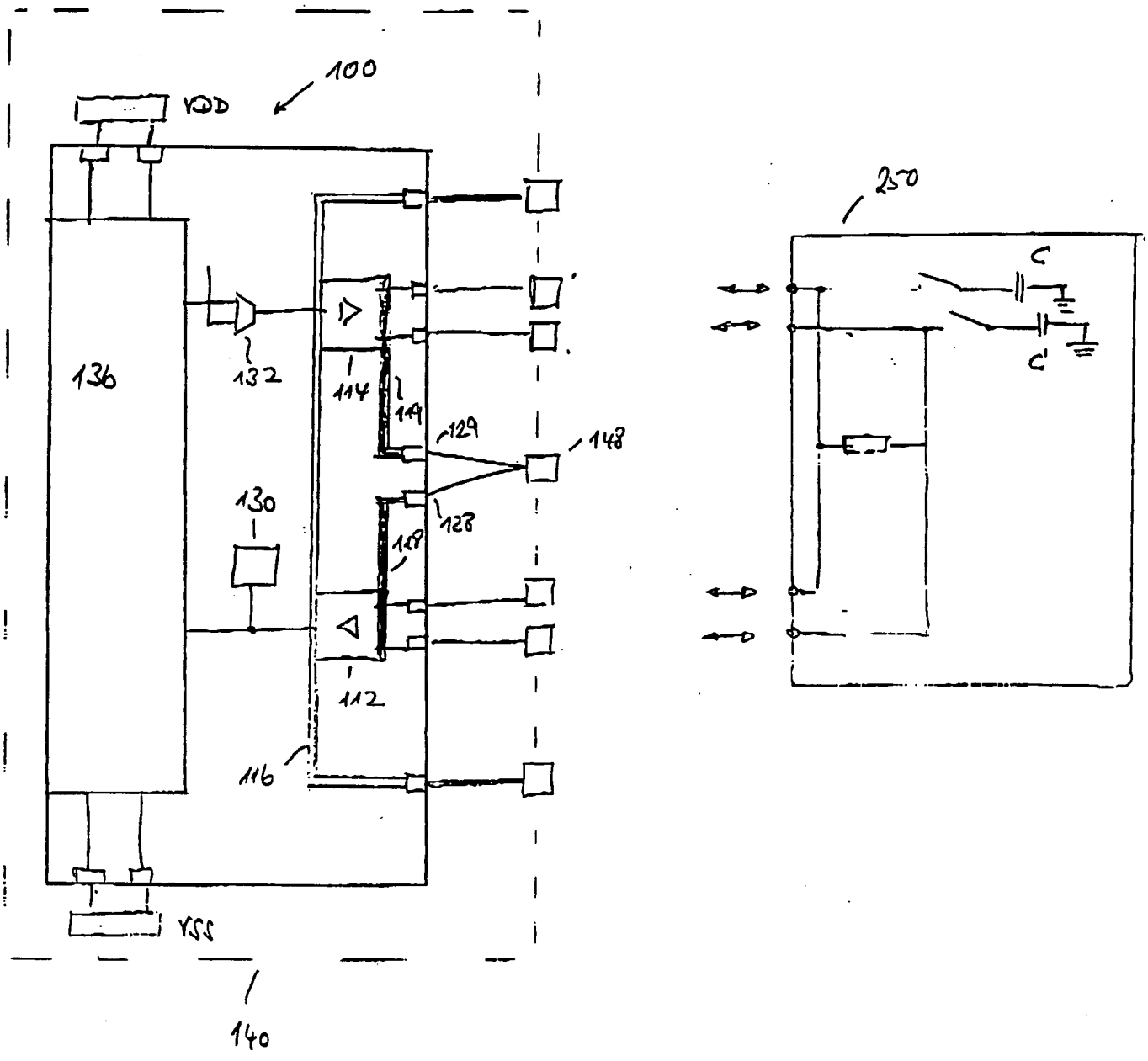
100
VDD
136
132
114
149
129
148
130
128
147
112
116
VSS
140
250
C
C'

Fig 3